ECE 312
Electronic Circuits (A)
Lec. 2: BJT Review

Instructor

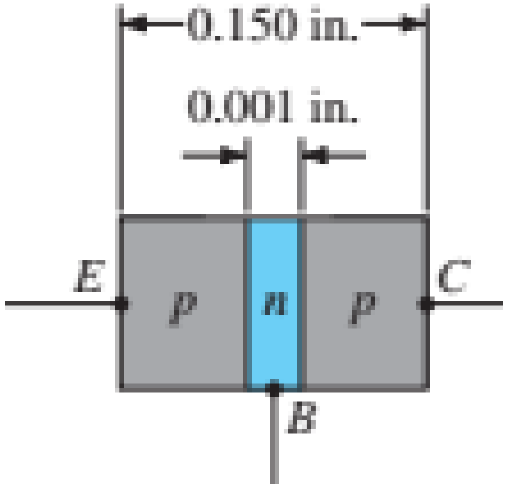
Dr. Maher Abdelrasoul

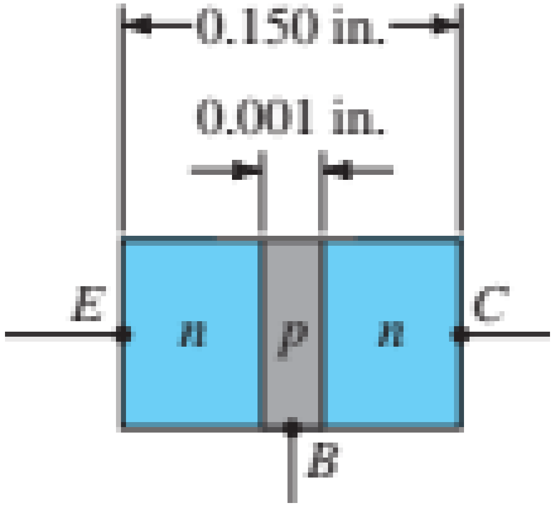
Outline

- Transistor Construction
- Transistor Operation
- Transistor Configuration

Transistor Construction

- The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material (npn transistor) or two *p*- and one *n*-type layers of material (pnp transistor).



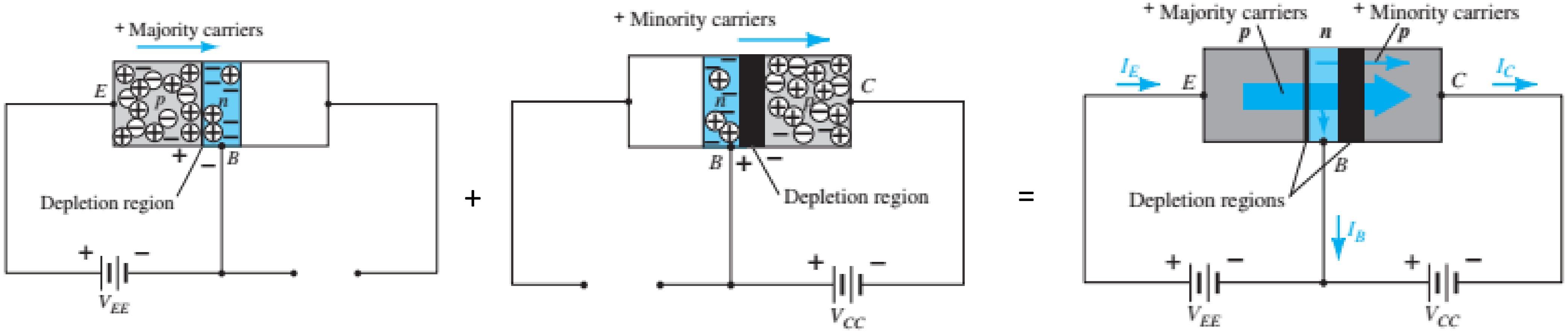


Transistor Operation

- The operation discussed in pnp transistor

One p–n junction of a transistor is reverse-biased,

whereas the other is forward-biased



- The collector current by Kirchhoff's law

$$I_E = I_C + I_B$$

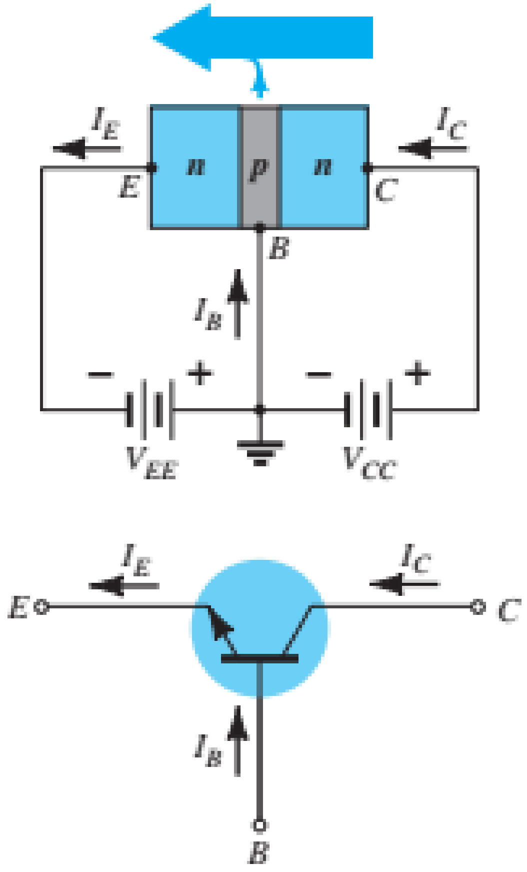
$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$

Transistor Configuration

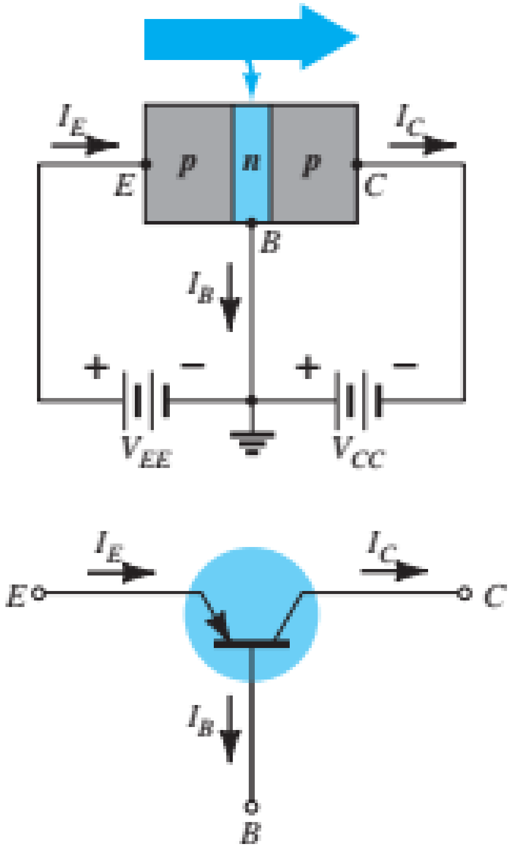
1. Common-Base Configuration
2. Common-Emitter Configuration
3. Common-Collector Configuration

1. Common-Base Configuration (1)

- The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration.

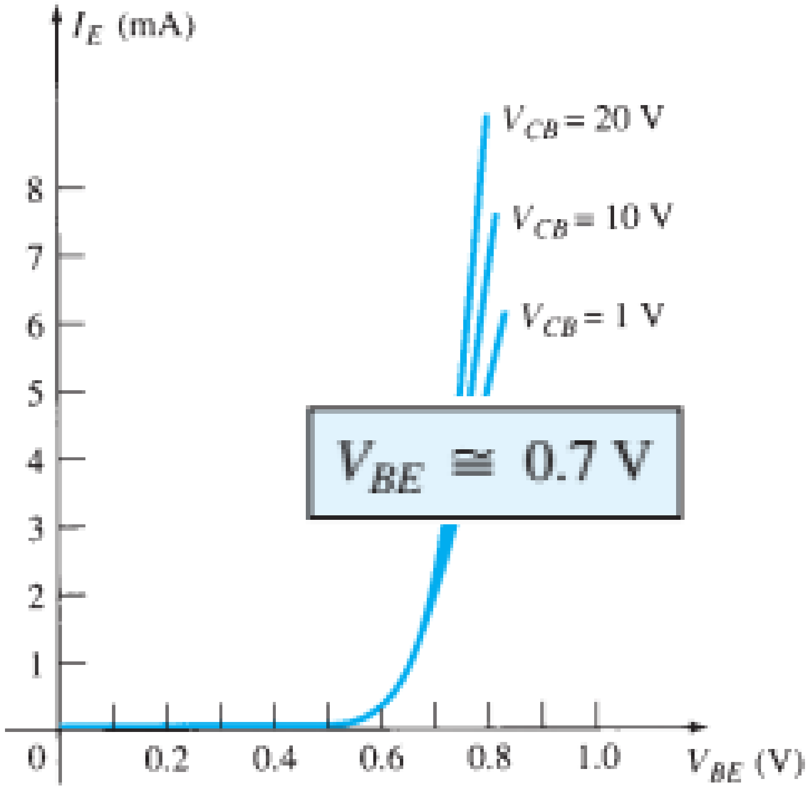


npn

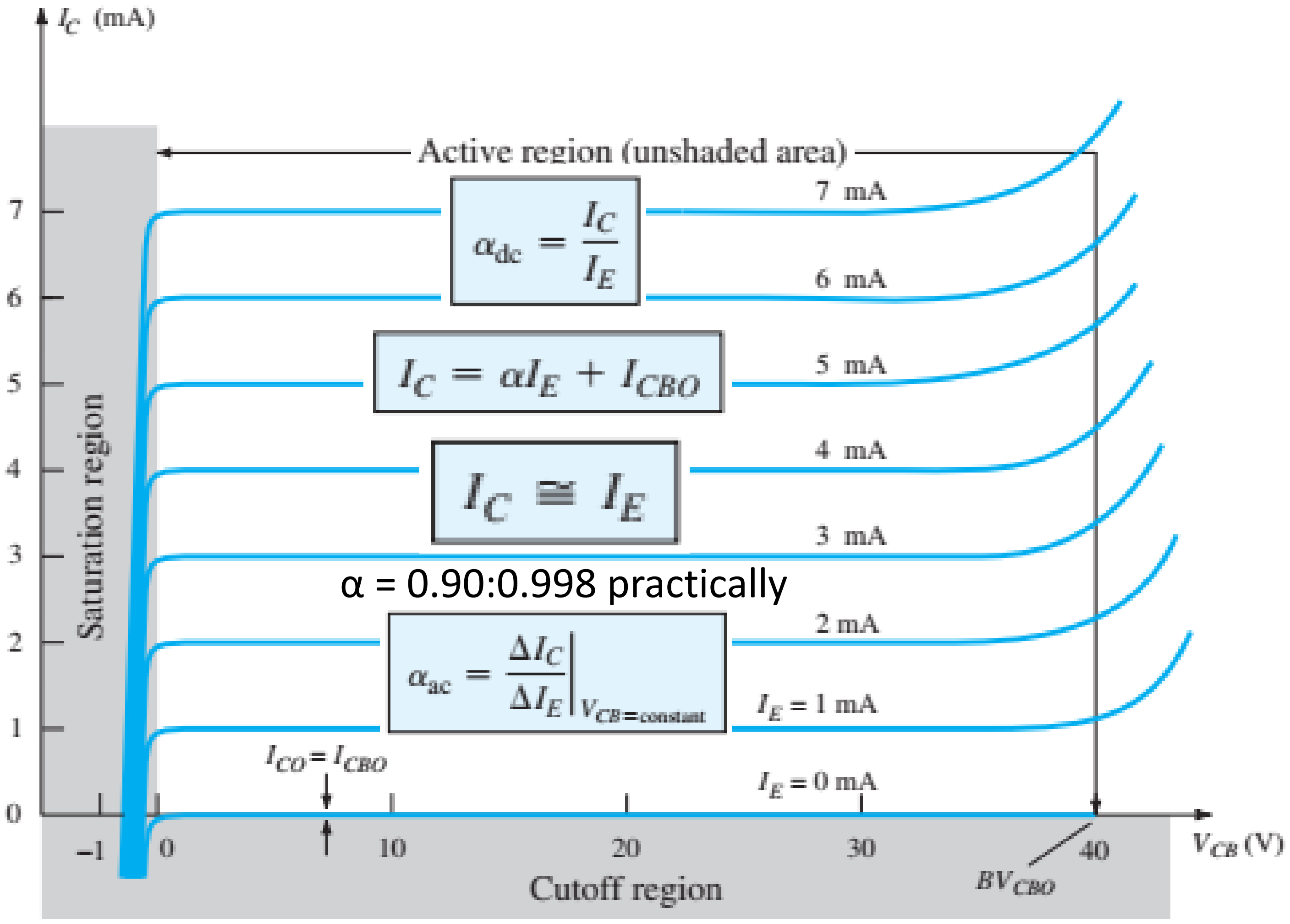


pnp

1. Common-Base Configuration (2)



Input or driving point characteristics for a common-base silicon transistor amplifier.

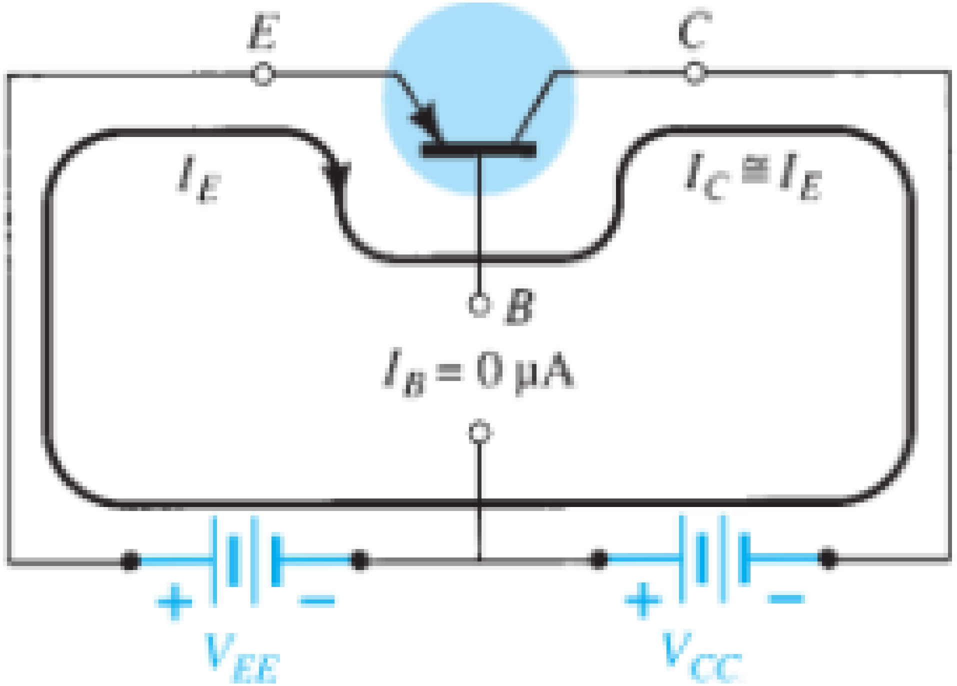


Output or collector characteristics for a common-base transistor amplifier.

1. Common-Base Configuration (3)

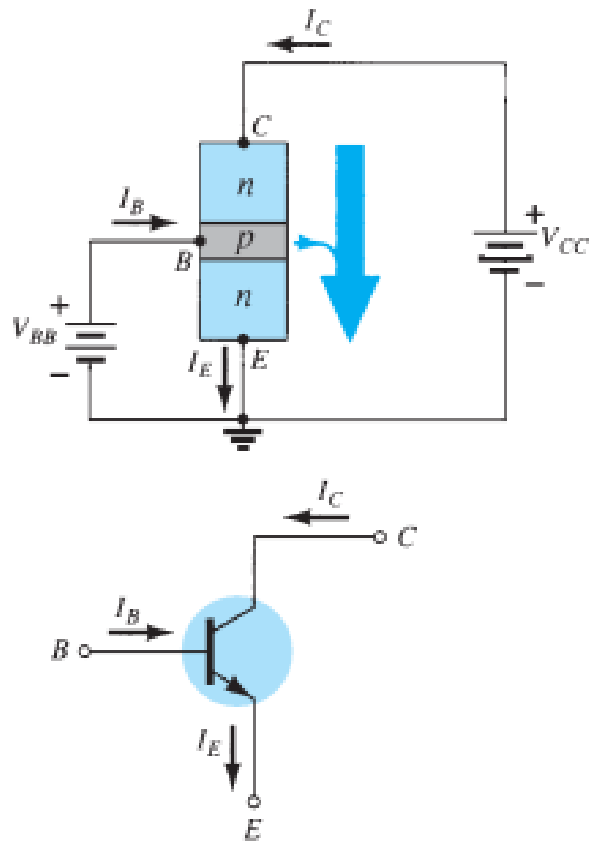
- Biasing of a CB pnp tr. in the active region:

In the active region the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.

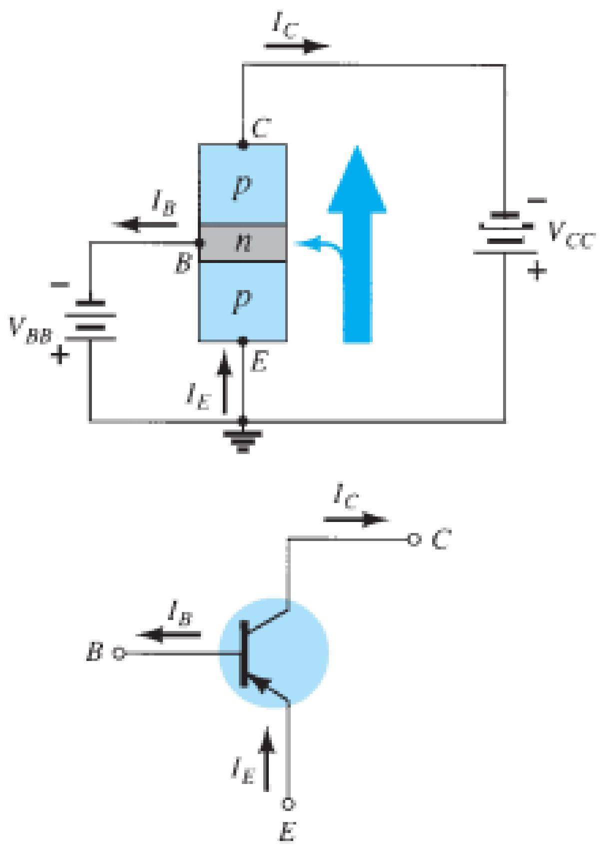


2. Common-Emitter Configuration (1)

- It is called the *common-emitter configuration* because the emitter is common to both the input and output terminals (in this case common to both the base and
collector terminals).

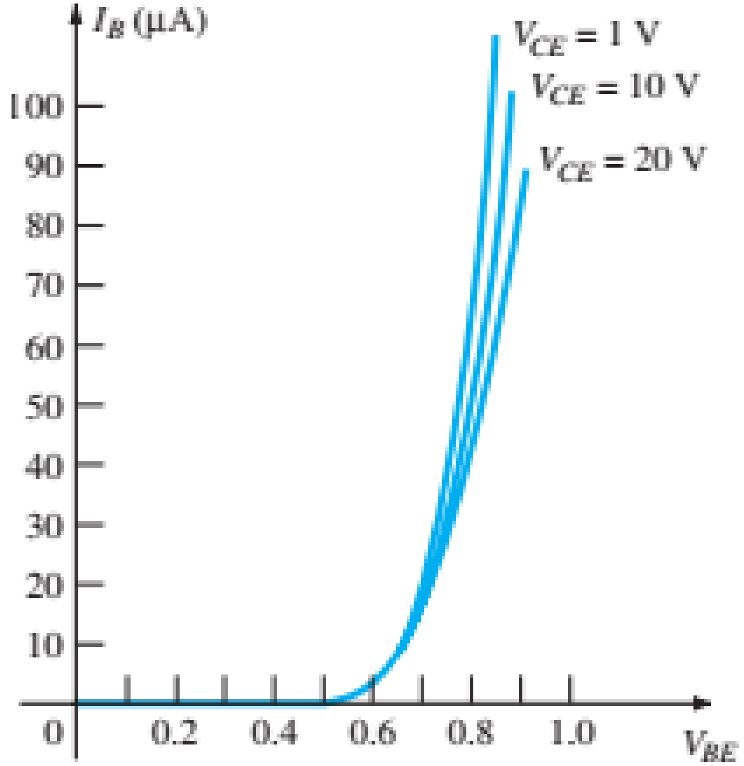


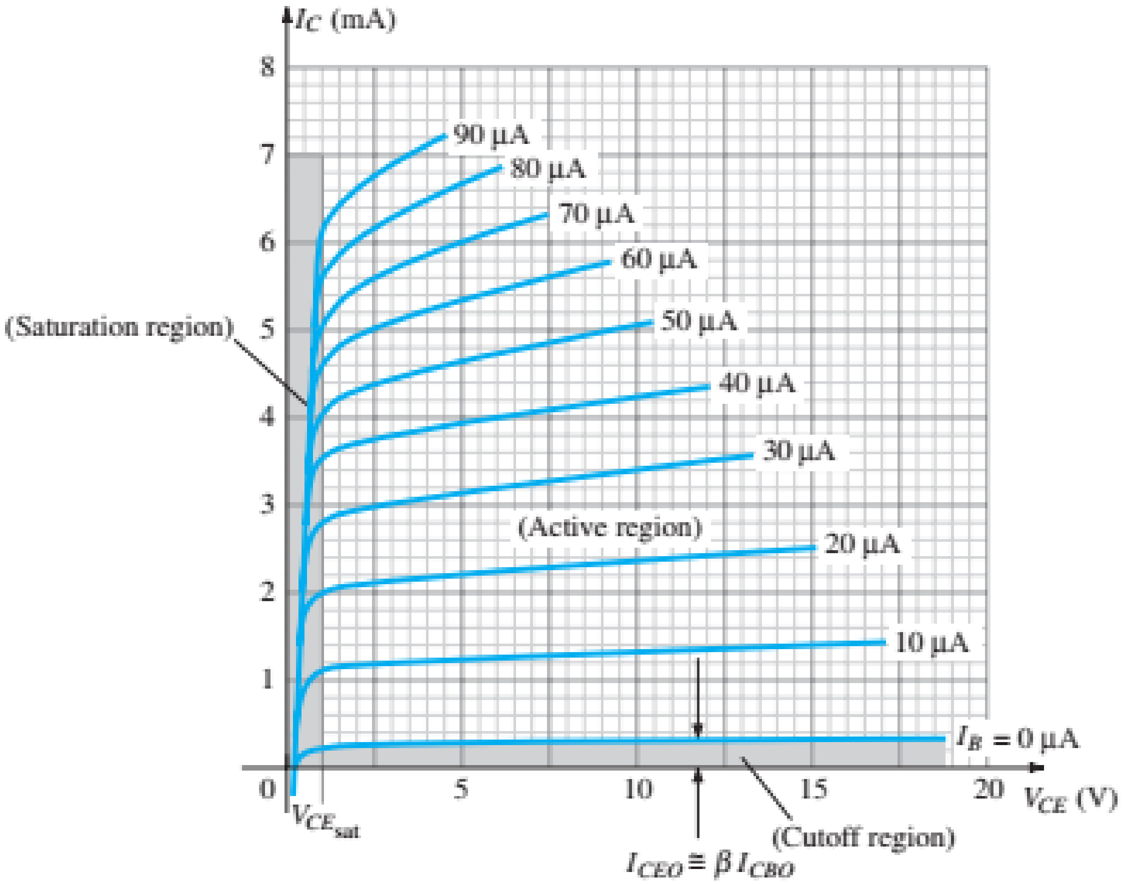
npn



pnp

2. Common-Emitter Configuration (2)





$$\beta_{dc} = \frac{I_C}{I_B}$$

β=50:400 practically

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

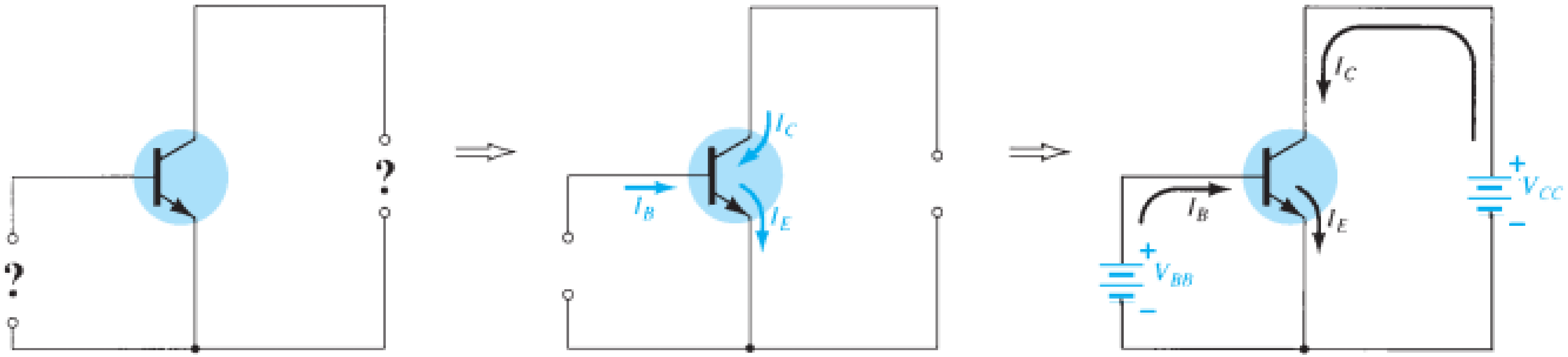
$$I_C = \beta I_B$$

$$I_E = (\beta + 1) I_B$$

2. Common-Emitter Configuration (3)

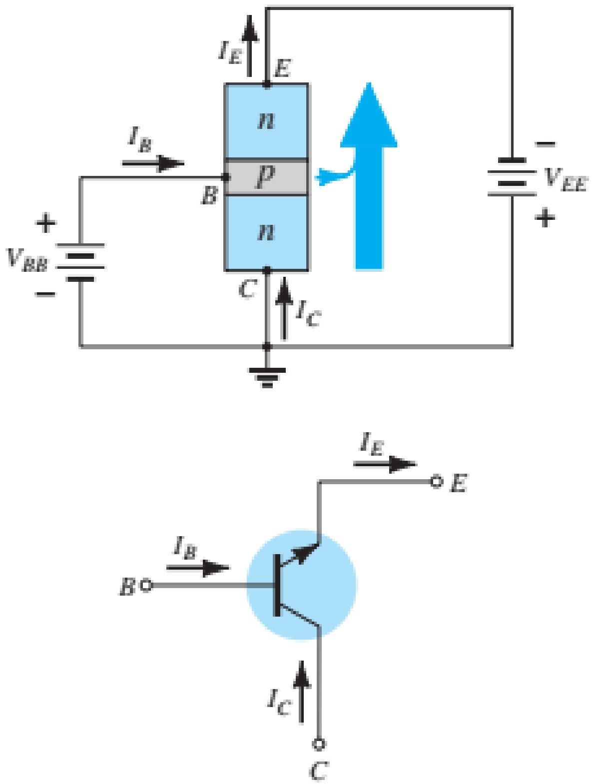
- Biasing of a CE npn tr. in the active region:

In the active region of a common-emitter amplifier, the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.

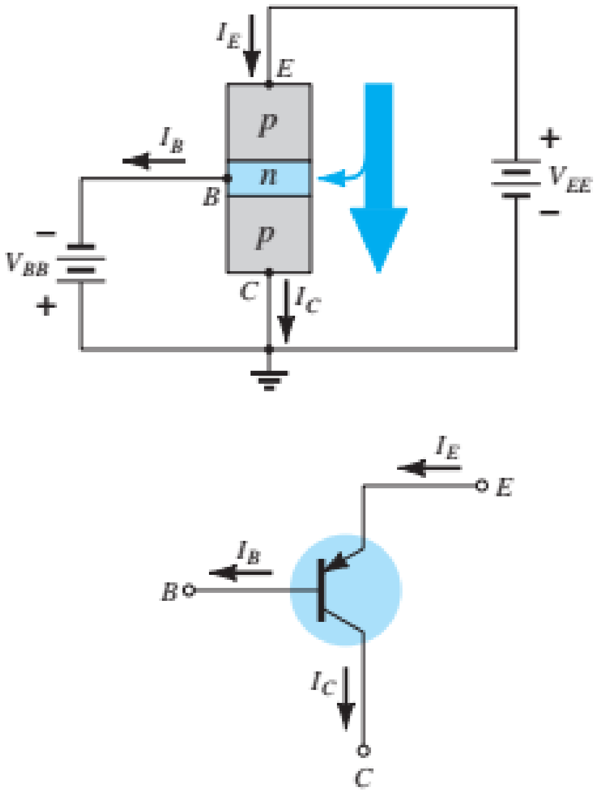


3. Common-Collector Configuration (1)

- The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common emitter configurations.



npn

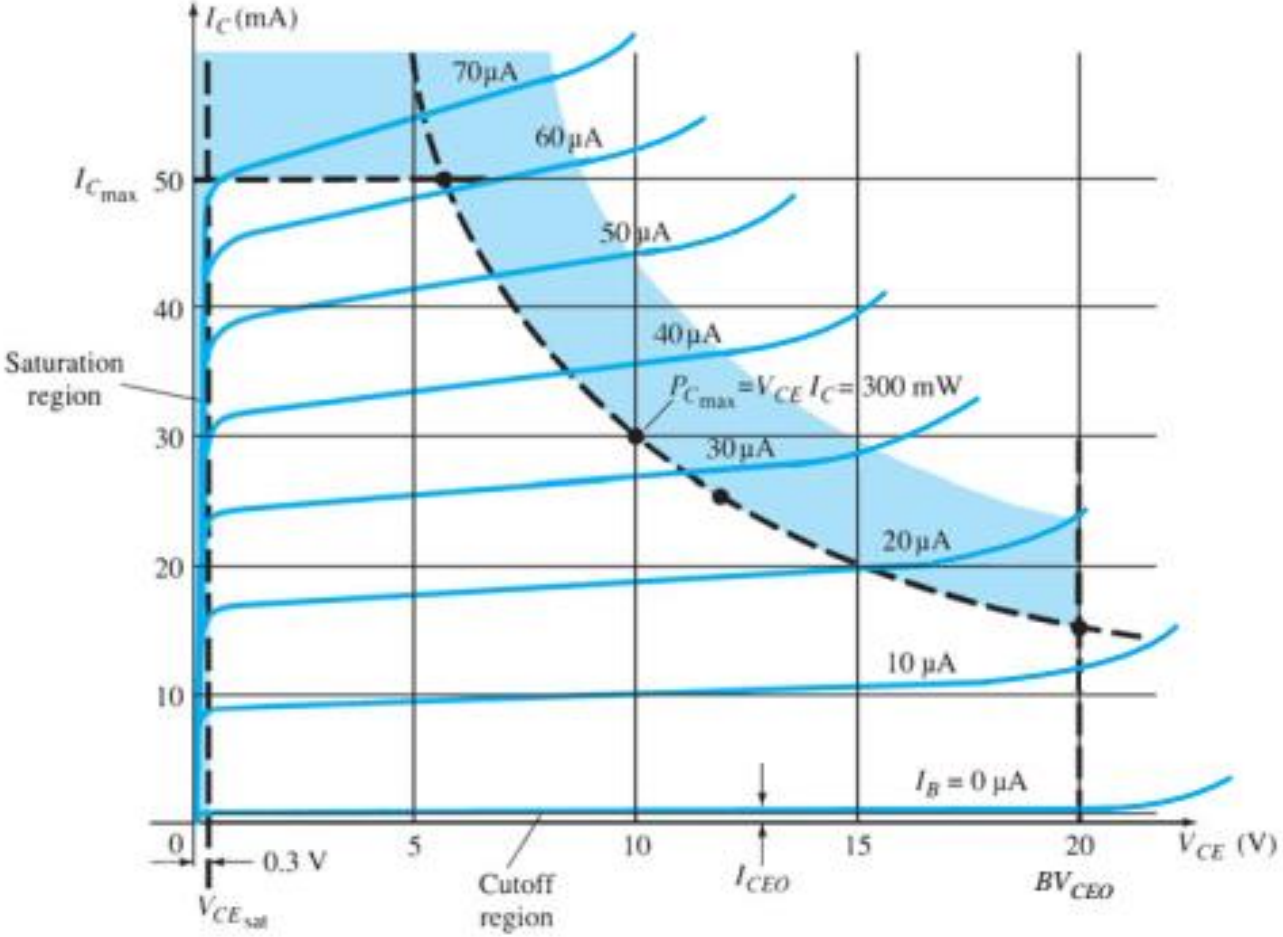


pnp

3. Common-Collector Configuration (2)

- Limits of operation

Defining the linear (undistorted) region of operation for a transistor



The output characteristics of the common-collector configuration are the same as for the common-emitter configuration ($I_c \approx I_E$).

$$P_{C_{max}} = V_{CE} I_C$$

$$I_{CEO} \leqq I_C \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq V_{CE} \leqq V_{CE_{max}}$$
$$V_{CE} I_C \leqq P_{C_{max}}$$

Transistor Configuration Summary

Configuration type	Current Gain	Voltage Gain	Power Gain	Input impedance	Output Impedance
Common Base	≈1	High	Average	Low	High
Common Emitter	High	High	High	Average	Average
Common Collector	High	≈1	Low	High	Low

Transistor Configuration Sheet

- Since the specification sheet is the communication link between the manufacturer and user, it is particularly important that the information provided be recognized and correctly understood.

OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0$ mAdc, $I_E = 0$)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage ($I_C = 10$ μAdc, $I_E = 0$)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage ($I_E = 10$ μAdc, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 20$ Vdc, $I_E = 0$)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current ($V_{BE} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) ($I_C = 2.0$ mAdc, $V_{CE} = 1.0$ Vdc) ($I_C = 50$ mAdc, $V_{CE} = 1.0$ Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{BE(sat)}$	–	0.95	Vdc
Small-Signal Current Gain ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, f = 1.0 kHz)	h_{fe}	50	200	–

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	−55 to +150	°C

Limits of Operation

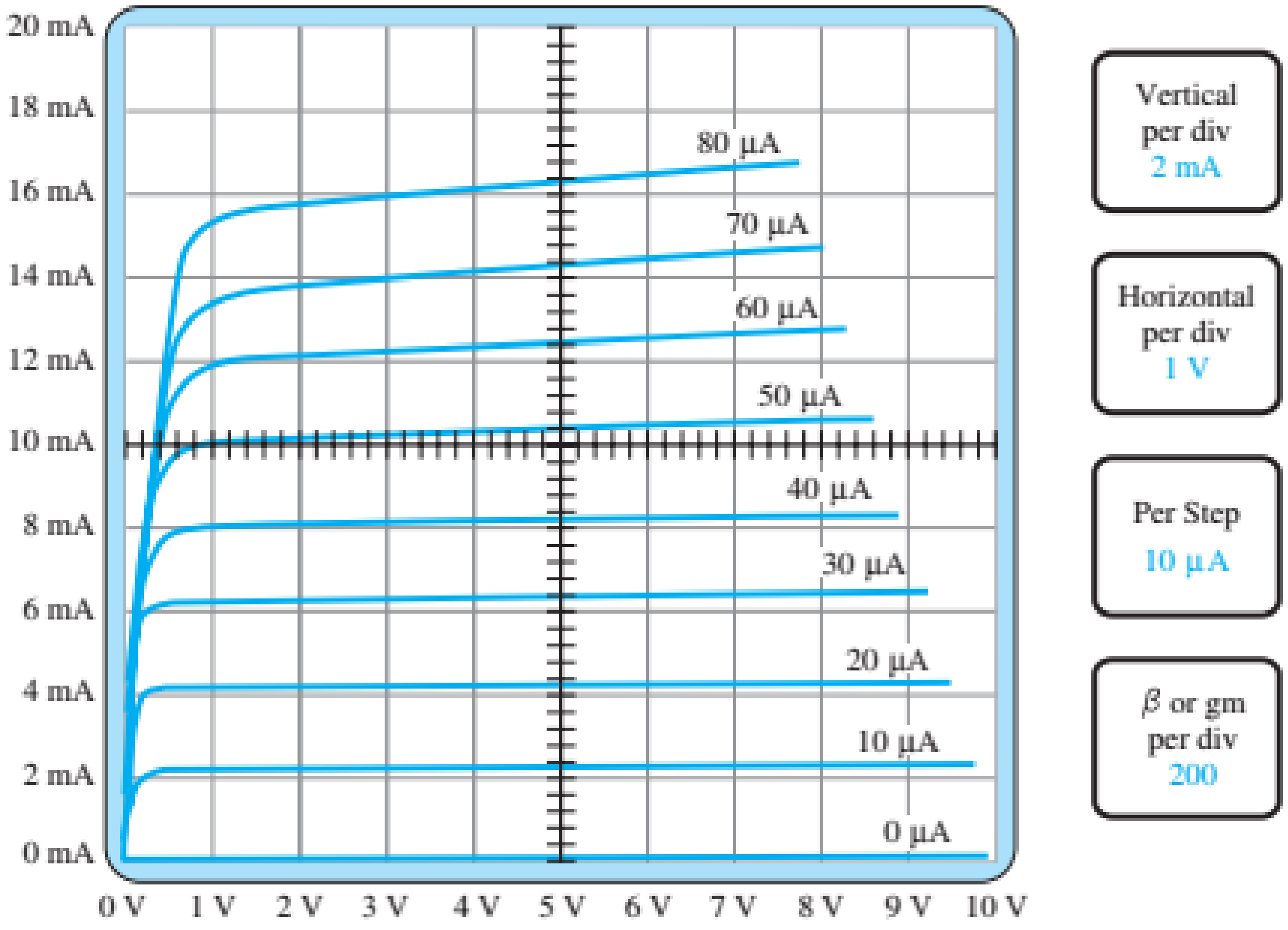
$$7.5\ \mu A \leqq I_C \leqq 200\ mA$$

$$0.3\ V \leqq V_{CE} \leqq 30\ V$$

$$V_{CE} I_C \leqq 650\ mW$$

Transistor Testing

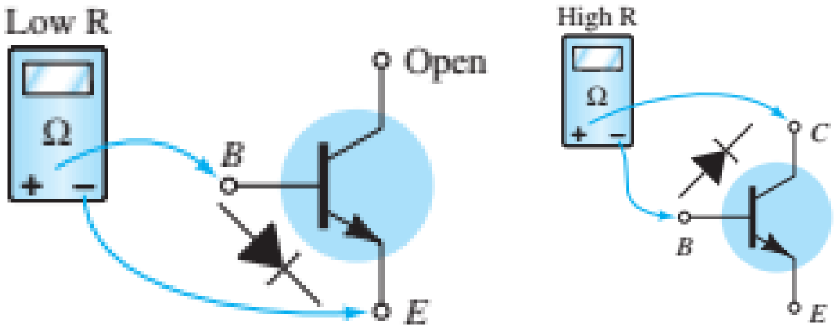
1. Curve Tracer



Curve tracer response to 2N3904 npn transistor.

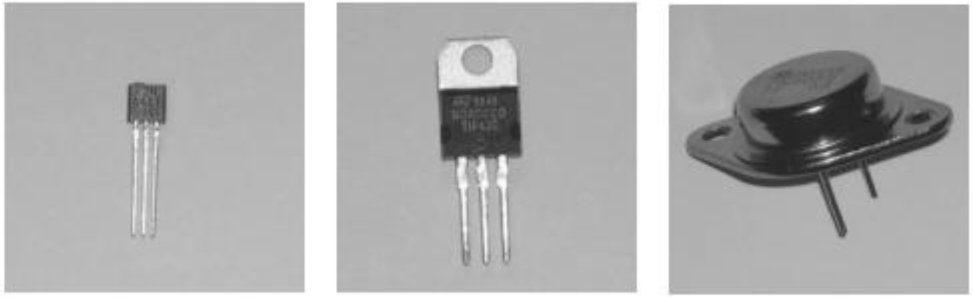
2. Transistor Testers

3. Ohmmeter



Transistor Casing and Terminal Identification

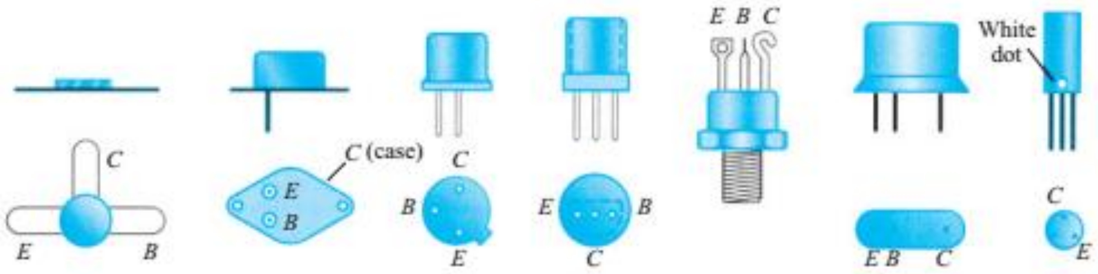
- Casing

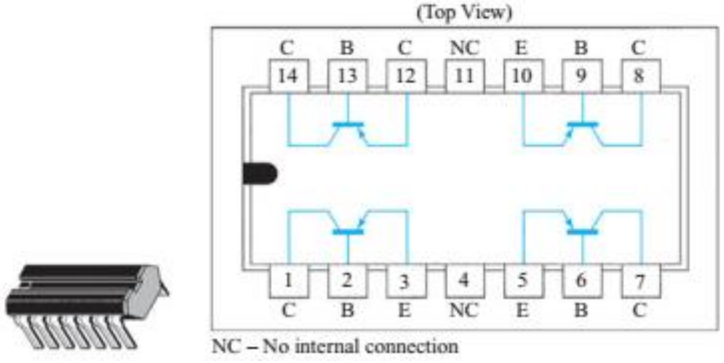


(a) (b) (c)

Various types of general-purpose or switching transistors:
(a) low power; (b) medium power; (c) medium to high power.

- Terminal Identification

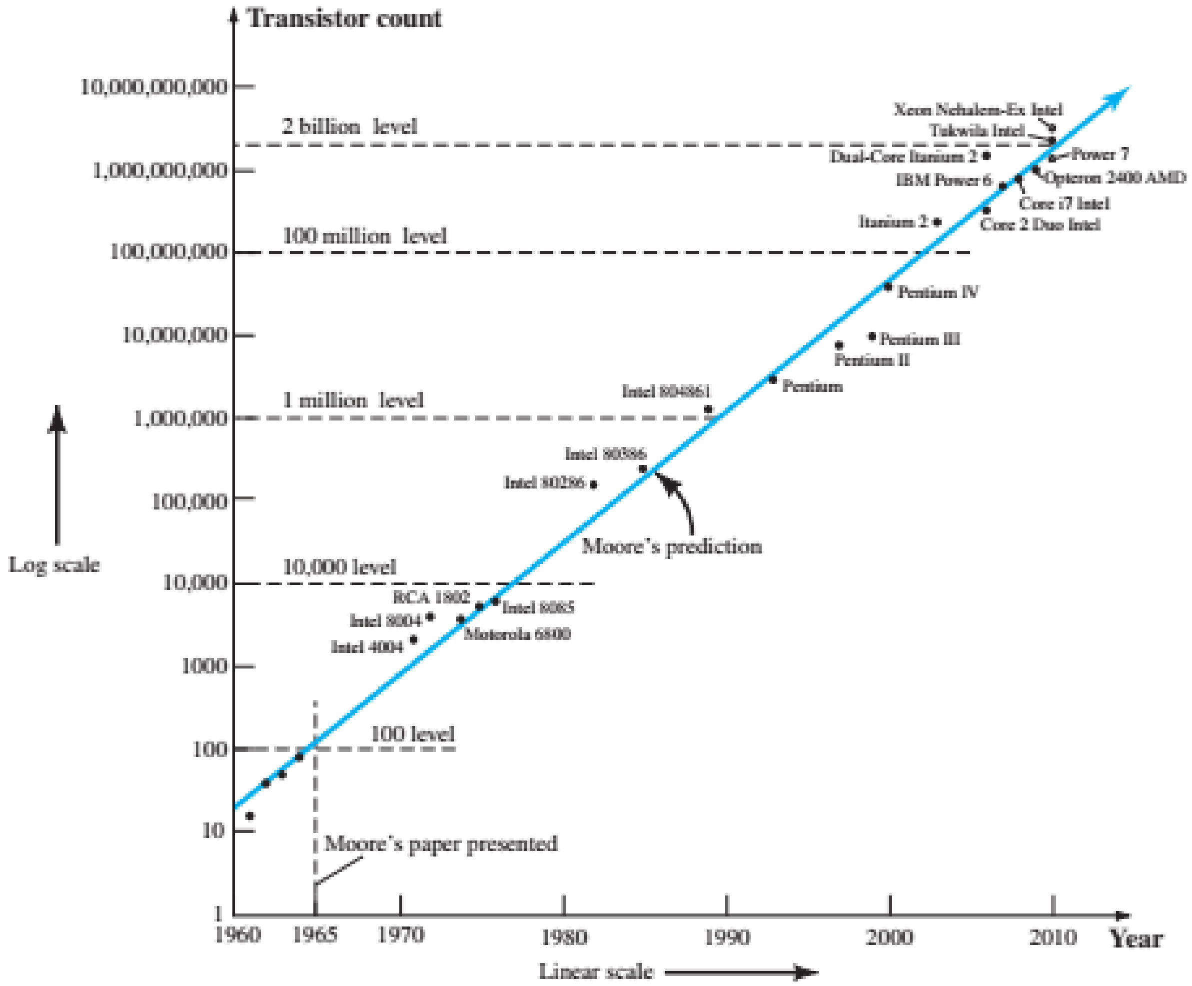




Type Q2T2905 Texas Instruments quad pnp silicon transistor

Transistor Development

- **Moore's law** predicts that the transistor count of an integrated circuit will double every 2 years.



Where can the field go from here?


Thank You!